request that a copy of each of the forms 1449, initialed by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Claims 28-38

The Examiner indicated that claims 28-38 were rejected, but did not indicate the nature of the rejection. The applicant respectfully requests that the Examiner clarify the status of claims 28-38 in the next office action.

Rejection under 35 USC §103

Claims 19-21 and 43-63 were rejected under 35 USC § 103(a) as being unpatentable over Sugita et al. (JP Patent No. 08-255878, Sugita) in view of Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata). The applicant respectfully traverses.

Claim 19 recites a method of using a floating gate transistor having a floating gate electrode and an adjacent amorphous silicon carbide (a-SiC) gate insulator between the floating gate electrode and a substrate.

Sugita is deficient in the following respects. Sugita discloses in Figure 1 a floating gate transistor with a source 2 and a drain 3 in a silicon substrate 1, and a floating gate 6 separated from the substrate 1 by a Beta-Silicon Carbide film 5. However, Sugita does not disclose an amorphous silicon carbide (a-SiC) gate insulator.

Sakata does not supply the elements missing in Sugita. Sakata does not disclose an electrode or a gate, and therefore does not disclose a gate insulator.

Sakata discloses in Figure 1 a diode structure comprising c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Column 3. Both a-SiC:H and a-Si:H are highly resistive, insulating layers. Both are hydrogenated to ensure high resistivity. A plot of capacitance-voltage (C-V) characteristics for the diode is shown in Fig. 2 of Sakata. The plot shows that the "capacitance at 3V (470pF) is in fairly good agreement with the calculated capacitance of stacked insulator layers." Column 2.

An electrode or a gate is known to those skilled in the art as a continuous, electrically conductive structure. Sakata is disclosing a diode structure comprised entirely of "stacked insulator layers", and does not disclose a continuous, electrically conductive structure.

Sakata discloses that both electrons and holes "can be stored in the a-Si:H layer because of the discontinuity of the conduction (valence) band edges at the a-SiC:H/a-Si:H interfaces." Column 1. However, Sakata has not substantially identified the mechanism for the charge storage: "We speculate that traps in the a-Si:H and/or at the interface between a-Si:H and a-SiC:H are acting as memory sites." Column 2. The band edges shown in Figure 1 are also pure speculation by Sakata: "However, we speculate that a band offset exists at both band edges in the present samples, as schematically shown in Fig. 1, because both electrons and holes are stored in the a-Si:H layer." Column 2. The storage mechanism in the diode structure disclosed by Sakata is a product of pure speculation, and therefore Sakata does not disclose an electrode or a gate.

The C-V plot shows a "large hysteresis" that may be used as a memory window. Column 2. While the hysteresis may be used to create a memory device, this does not imply that the diode structure has an electrode or a gate. The diode structure of Sakata is comprised entirely of alternate layers of highly resistive insulators, and does not include an electrode or a gate. Therefore, Sakata does not disclose a gate insulator.

Furthermore, there is no suggestion in either Sugita or Sakata for the combination put forward by the Examiner.

There must be a showing of a "teaching or motivation to combine prior art references" to support a rejection under section 103 and "the showing must be clear and particular." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Such a showing of a "teaching or motivation to combine" is necessary to avoid the use of hindsight when combining references under section 103. 50 USPQ2d at 1616-17.

The diode structure of Sakata and the floating gate transistor of Sugita are fundamentally different. The diode structure of Sakata is comprised entirely of alternate layers of highly resistive insulators, and does not include an electrode or a gate. The floating gate transistor of Sugita is a traditional floating gate transistor with a source and a drain in a silicon substrate and a floating gate separated from the substrate by an insulator. Sakata has only speculated on the reasons for the performance of the diode structure. The operation of a floating gate transistor is

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well known. The Examiner has not identified a suggestion in either Sakata or Sugita for combining the two different structures.

Therefore, the applicant respectfully submits that claim 19 is not disclosed or suggested by Sugita and Sakata. Claims 20-21 and 43-63 recite elements similar to those recited in claim 19. For reasons analogous to those state above, and the limitations in the claims, the applicant respectfully submits that claims 20-21 and 43-63 are also not disclosed or suggested by Sugita and Sakata.

New Claims

The applicant has added new claims 64-75, and respectfully submits that all of the new claims 64-75 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,
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Date 10 MAR 2000 By _____
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **March 10, 2000.**

JANA OTOMAR
Name

Jana D. Otomar
Signature

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